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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,627	07/15/2004	Nicolas Guillarme	026032-4787	4873

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EXAMINER	
KAPLAN, HAL IRA	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,627	GUILLARME ET AL.	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-21,23-25,27,28 and 30-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11,13-21,23-25,27,28 and 30-36* is/are allowed.

6)☒ Claim(s) *1,4 and 5* is/are rejected.

7)☒ Claim(s) *3 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US patent of Carpenter et al. (6,275,958) in view of the US patent of Hemena et al. (6,160,386), and further in view of the US patent of Mitchell (4,412,277).

As to claim 1, Carpenter, drawn to fault detection in a redundant power converter, discloses, in Figures 5 and 6, a DC/DC voltage converter comprising: a first positive terminal (+Vin) and a first negative terminal (ground) for connection respectively to two terminals of a high-voltage electrical network; a second positive terminal (+Vout) and a second negative terminal (ground) for connection respectively to two terminals of a low-voltage electrical network (see column 1, lines 25-28); and n cells (20) connected in parallel, where n is an integer greater than unity, disposed between the first positive (+Vin) and negative (ground) terminals and between the second positive (+Vout) and negative (ground) terminals, each cell (20) comprising a chopper DC/DC converter (see column 2, lines 8-10 and 64-67, and Figure 6), each having a first circuit branch (ground) interconnecting the first and second negative terminals, a second circuit branch including an inductor (19) and interconnecting the first (+Vin) and second (+Vout) positive terminals, chopper means comprising at least one chopper switch (S1), and a management unit (18) adapted to control OFF and ON switching of the chopper switch (S1) with a determined duty ratio (see column 1, lines 37, 46-51, and 60-63, and Figure 6). Carpenter does not disclose only one protection transistor, or the intrinsic diode of the transistor connected to the inductor by its cathode and to the second positive terminal by its anode.

Hemena, drawn to a parallel power system which includes over voltage protection, discloses, in Figure 3B, a DC/DC converter cell comprising a single protection transistor (102) (see column 2, lines 54-55 and column 3, lines 10-13 and 38-44). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the DC/DC converter of Carpenter using cells comprising a single protection transistor as taught by Hemena, in order to reduce the number of parts and the cost.

Mitchell, drawn to an AC-DC converter having an improved power factor, discloses a MOS transistor (17) connected in series with an inductor (9), and including an intrinsic diode (21) connected to the inductor by its cathode (see column 2, lines 31-33 and Figure 1). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use a MOS transistor connected in series between the inductor and second positive terminal of Carpenter, and including an intrinsic diode connected to the inductor by its cathode and to the second positive terminal by its anode, in order to prevent current flow to the load (CPU) when there is supposed to be no load current.

As to claim 4, in the converter of Hemena, the single protection transistor (102) in each cell (100(a)) is connected in a high-voltage portion of the cell (see Figure 3B).

As to claim 5, the protection transistor of Hemena is a MOS transistor (Q2) connected in series in the second circuit branch so as to be immediately adjacent to the first positive terminal (Vin) (see Figure 3B). The converter of Carpenter teaches a MOS protection transistor (48) connected in series in the second circuit branch so as to be immediately adjacent to the first positive terminal (+Vin), with an intrinsic diode

connected to the first positive terminal by its cathode (see column 4, lines 48-51 and Figure 5). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the converter of Carpenter in view of Hemena, as set forth above, with the MOS protection transistor of Carpenter in place of the MOS protection transistor (102) of Hemena, in order to block an overvoltage resulting from a short of the MOS protection transistor.

Allowable Subject Matter

5. Claims 7-11, 13-21, 23-25, 27, 28, and 30-36 allowed.

6. Claims 3 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Claims 3 and 6 contain allowable subject matter because none of the prior art of record teaches or discloses both a single protection transistor in each cell and a protection switch which is common to all of the cells, in combination with the remaining claimed features.

8. The following is an examiner's statement of reasons for allowance:

Claims 7-11, 13-21, 23-25, 27, and 28 are allowed because none of the prior art of record discloses or suggests both a single protection transistor in each cell and a protection switch which is common to all of the cells, in combination with the remaining claimed features.

Claims 30-36 are allowed because none of the prior art of record discloses the components that are dedicated to a protection function giving rise to static consumption of power less than 0.5% of the total static consumption of the converter, in combination with the remaining claimed features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

9. Applicant's arguments, see Remarks, filed November 14, 2006, with respect to the objections have been fully considered and are persuasive. The objections have been withdrawn. The rejection of claim 29 is moot because claim 29 has been cancelled.

10. As to claims 1, 4, and 5, as to Applicant's arguments that Hemena et al. do not teach a single protection transistor disposed in a circuit branch including an inductor and interconnecting the first and second positive terminals, and that Mitchell et al. do not teach a DC/DC converter, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It would have been obvious to one of ordinary skill in the art to use only a single protection transistor, as taught by Hemena et al., instead of

two protection transistors, as taught by Carpenter et al., in order to use fewer parts and thus reduce the cost of the device. The Examiner agrees that Mitchell et al. do not teach a DC/DC converter, but Carpenter et al. and Hemena et al. do teach a DC/DC converter, as set forth above.

As to Applicant's argument that the MOS transistors of Mitchell do not perform any protective function, the Examiner agrees; however, Mitchell was cited only for the specific connection of a transistor (17) connected in series with an inductor (9), and not for the function of the transistor, which is disclosed by Carpenter et al. The diode is intrinsic to the transistor (17) and is thus by definition connected in parallel with the transistor. It appears that the Applicant may have misunderstood the rejection to refer to the extrinsic diode (13) of Mitchell; however, this extrinsic diode is not relevant to the rejection.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hik

ROBERT L. DEBERADINIS
PRIMARY EXAMINER